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Enclosed is a complete human translation of Japanese Patent 2000-68620 which was recently received by the examiner. Any further communication directed to this application can be directed to Jeff Aftergut at 571-272-1212.

Jeff H. Aftergut
Primary Examiner
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CIRCUIT BOARD AND MANUFACTURING METHOD THEREFOR
[Kairo kiban oyobi sono seizo hoho]

Yasuhiro Nakaya, et al.

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[Claims] /2*

[Claim 1] A circuit board having an insulating layer with through-holes formed therein, a conductive composition filling the through-holes, and a wiring pattern formed on both sides of the insulating layer, wherein the wiring pattern formed on both sides of the insulating layer is connected electrically via the conductive composition, and wherein at least one interface between the wiring pattern and the conductive composition is coarser than the interface with the insulating layer.

[Claim 2] A method for manufacturing a circuit board comprising a step in which metal foil is laminated on one side of the insulating layer and a resin film is laminated on the other side, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is coarsened, and a step in which the holes are filled with a conductive composition.

[Claim 3] A method for manufacturing a circuit board comprising a step in which an insulating layer and resin film are laminated in this order on the surface of a core layer in which a metal foil wiring pattern has been formed, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the

* Number in the margin indicates pagination in the foreign text.

bottom surface of the holes is coarsened, and a step in which the holes are filled with a conductive composition.

[Claim 4] A circuit board having an insulating layer with through-holes formed therein, a conductive composition filling the through-holes, a wiring pattern formed on both sides of the insulating layer, and a conductive buffer layer disposed between the wiring pattern and the conductive composition, wherein the wiring pattern formed on both sides of the insulating layer is connected electrically via the conductive composition and the conductive buffer layer, and wherein at least one interface between the wiring pattern, the conductive buffer layer and the conductive composition is coarser than the interface with the insulating layer.

[Claim 5] The circuit board described in Claim 4, wherein bumps are added to the conductive buffer layer at the interface with the conductive composition and/or wiring pattern.

[Claim 6] The circuit board described in Claim 4, wherein the conductive buffer layer is a metal or alloy compound formed with the metal component contained in the conductive composition and/or wiring pattern.

[Claim 7] A method for manufacturing a circuit board comprising a step in which metal foil is laminated on one side of the insulating layer and a resin film is laminated on the other side, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is

coarsened, a step in which a conductive buffer layer is formed on the coarsened bottom surface of the holes, and a step in which the holes are filled with a conductive composition.

[Claim 8] A method for manufacturing a circuit board comprising a step in which an insulating layer and resin film are laminated in this order on the surface of a core layer in which a metal foil wiring pattern has been formed, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is coarsened, a step in which a conductive buffer layer is formed on the coarsened bottom surface of the holes, and a step in which the holes are filled with a conductive composition.

[Claim 9] The circuit board manufacturing method described in Claims 2, 3, 7 or 8, wherein the method used to coarsen the surface of the metal foil includes abrasive finishing.

[Claim 10] The circuit board manufacturing method described in Claims 2, 3, 7 or 8, wherein the method used to coarsen the surface of the metal foil includes partial removal or plastic deformation of the metal foil.

[Claim 11] The circuit board described in Claims 1, 4, 5 or 6, wherein the conductive composition contains as a filler at least one metal selected from among gold, silver, copper, nickel and palladium or an alloy thereof, and wherein the wiring pattern is copper or an alloy whose main component is copper.

[Claim 12] The circuit board described in any one of Claims 4 through 6, wherein the conductive buffer layer is at least one metal selected from among gold, silver, tin, zinc, indium and palladium or an alloy or metal compound thereof.

[Claim 13] The circuit board described in any one of Claims 4 through 6, wherein the thickness of the conductive buffer layer is greater than 0.01 μm and less than 20 μm.

[Claim 14] The circuit board described in Claims 1, 4, 5, 6, 11, 12 or 13, wherein a resistor composition or thermally conductive composition is used instead of a conductive composition.

[Claim 15] The circuit board manufacturing method described in Claims 2, 3, 7, 8, 9 or 10, wherein a resistor composition or thermally conductive composition is used instead of a conductive composition.

[Detailed Description of the Invention]

[0001] [Field of the Invention]

The present invention relates to a circuit board and manufacturing method therefor.

[0002] [Prior Art]

As electronic devices become smaller and more high performance, circuit boards with more layers and greater density are required. Higher density is achieved using inner via holes (IVH) in interlayer connections between boards where integrated circuits and components can be bonded via the shortest distance.

[0003] In multi-layer boards with IVH connections, a circuit board connecting material such as a prepreg filled "in via" with a conductive resin composition (a paste or conductive paste) is laminated on a core material with a pattern formed beforehand consisting of copper foil for pattern formation. This is heated and pressed using the heat press method to complete the board.

[0004] The conductive paste consists of a conductive filler such as copper powder dispersed in a synthetic resin binder such as an epoxy resin. This fills the through-holes formed at predetermined locations in a prepreg with peelable film on both sides using a method, such as printing. /3

[0005] In the heating/pressing step, the binder in the conductive paste adheres to the conductive filler and copper foil for circuit formation to manifest mechanical strength and obtain an IVH connection through mechanical contact between the conductive filler and the copper foil.

[0006] [Problem Solved by the Invention]

However, in the prior art IVH connection technique, the conductive filler and copper foil are simply brought into contact with each other. As a result, the electrical connection is unreliable. Circuit boards for semiconductor packages such as LSIs and module applications (MCM, CSP, etc.) require a high degree of reliability. When a pressure cutter test (PCT) is conducted, there is high connection resistance at the conductive composition/copper foil interface "in via" and shorts occur in extreme cases.

[0007] IVH connection reliability is very important to the performance of multi-layer boards. IVH connection resin multi-layer boards must be improved if they are to be used in semiconductor packages and module applications as they become more dense and lightweight.

[0008] The purpose of the present invention is to solve this problem by providing a circuit board and manufacturing method therefor for realizing a circuit board with highly reliable IVH connections.

[0009] [Means of Solving the Problem]

In order to achieve this purpose, the present invention has the following configuration.

[0010] The first invention is a circuit board having an insulating layer with through-holes formed therein, a conductive composition filling the through-holes, and a wiring pattern formed on both sides of the insulating layer, wherein the wiring pattern formed on both sides of the insulating layer is connected electrically via the conductive composition, and wherein at least one interface between the wiring pattern and the conductive composition is coarser than the interface with the insulating layer.

[0011] Because the contact interface between the conductive composition and the wiring pattern is coarsened in the first configuration, the contact area is increased, the number of contact points between the conductive filler in the conductive composition and the wiring pattern is increased, the adhesive strength between the

resin in the conductive composition and the wiring pattern is increased, and the connection reliability is improved.

[0012] Because the coarsened region of the wiring pattern is limited to the connection interface with the conductive composition in the first configuration, fine pattern formation in the wiring pattern is easier than when the entire surface is coarsened. In circuit boards where fully coarsened metal foil is laminated on an insulating layer, the coarsened portion has to be deeply embedded in the insulating layer when the metal foil is etched for circuit pattern formation. This requires over etching, which makes improved pattern precision difficult.

[0013] The second configuration is a method for manufacturing a circuit board comprising a step in which metal foil is laminated on one side of the insulating layer and a resin film is laminated on the other side, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is coarsened, and a step in which the holes are filled with a conductive composition.

[0014] The third configuration is a method for manufacturing a circuit board comprising a step in which an insulating layer and resin film are laminated in this order on the surface of a core layer in which a metal foil wiring pattern has been formed, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the

surface of the metal film at the bottom surface of the holes is coarsened, and a step in which the holes are filled with a conductive composition.

[0015] With the second or third configuration, the circuit board in the first configuration can be manufactured efficiently.

[0016] The fourth configuration is a circuit board having an insulating layer with through-holes formed therein, a conductive composition filling the through-holes, a wiring pattern formed on both sides of the insulating layer, and a conductive buffer layer disposed between the wiring pattern and the conductive composition, wherein the wiring pattern formed on both sides of the insulating layer is connected electrically via the conductive composition and the conductive buffer layer, and wherein at least one interface between the wiring pattern, the conductive buffer layer and the conductive composition is coarser than the interface with the insulating layer.

[0017] In the fourth configuration, a conductive buffer layer is formed between the wiring pattern and the conductive composition, and the contact interface between the wiring pattern and the conductive buffer layer are coarsened. This increases the contact area. The conductive buffer layer adds surface bumps to the wiring pattern, which increases adhesiveness and makes it easier to form an alloy or metal compound with the metal component of the wiring pattern. By forming a very thin conductive buffer layer, the unevenness of the coarsened wiring pattern is applied to the surface of the conductive buffer layer. As a result, the contact interface between the

conductive buffer layer and the conductive composition is coarsened, the contact area is increased, the unevenness of the conductive filler in the conductive composition is applied to the conductive buffer layer, the adhesive properties are improved, an alloy or metal compound can be formed with the metal component constituting the conductive filler, and the adhesive strength between the resin in the conductive composition and the conductive buffer layer is improved. As a result, the reliability of the connections between the wiring pattern and the conductive composition is improved.

[0018] In the fourth configuration, the coarsened region of the wiring pattern is restricted to the connection interface with the conductive buffer layer. As in the circuit board in the first /4
configuration, fine formation of the wiring pattern is easier than when the entire surface is coarsened.

[0019] The fifth configuration is a method for manufacturing a circuit board comprising a step in which metal foil is laminated on one side of the insulating layer and a resin film is laminated on the other side, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is coarsened, a step in which a conductive buffer layer is formed on the coarsened bottom surface of the holes, and a step in which the holes are filled with a conductive composition.

[0020] The sixth configuration is a method for manufacturing a circuit board comprising a step in which an insulating layer and resin

film are laminated in this order on the surface of a core layer in which a metal foil wiring pattern has been formed, a step in which through-holes are formed from the resin film side to the interface between the metal foil and insulating layer, a step in which the surface of the metal film at the bottom surface of the holes is coarsened, a step in which a conductive buffer layer is formed on the coarsened bottom surface of the holes, and a step in which the holes are filled with a conductive composition.

[0021] With the fifth or sixth configuration, the circuit board in the fourth configuration can be manufactured efficiently.

[0022] In the configurations related to the circuit board manufacturing methods, the coarsening of the surface of the metal foil constituting the wiring pattern preferably includes abrasive finishing, partial removal of the metal foil or plastic deformation. These preferred configurations make coarsening of the metal foil surface more efficient.

[0023] [Embodiment of the Invention]

The following is an explanation of the circuit board and manufacturing method therefor in the present invention with reference to the drawings.

[0024] (1st Embodiment)

Fig. 1 shows the circuit board configuration in the first embodiment where (a) is a cross-sectional view and (b) is an enlarged cross-sectional view of section A in (a).

[0025] In Fig. 1, 1 denotes the insulating layer which is a board consisting of an aramid unwoven fabric impregnated with epoxy resin (prepreg sheet), 2 denotes the conductive composition filling the through-holes in the insulating layer [1] which is a conductive paste consisting of copper powder mixed in with epoxy resin, and 3 denotes the metal foil constituting the wiring pattern which is copper foil.

[0026] The interface between the conductive paste [2] and the copper foil [3] laminated on the outer surface of the outermost insulating layers [1a, 1b] is coarsened as shown in (b). In this figure, only the connection interface of the copper foil on the outermost layer necessary for land strength is coarsened, but the connection interface on the inner layers can be similarly coarsened. The effect is significant when used on the shiny surfaces of the copper foil on the inner layers.

[0027] The conductive composition is generally used to fill the via holes. This can consist of 80 to 95 wt% metal powder (filler) of at least one metal selected from among gold, silver, copper, nickel and palladium or an alloy thereof with an average grain diameter of 0.5 to 20 μm, and 5 to 20 wt% binder (whose main component is at least one synthetic resin selected from among epoxy resin, phenol resin, polyimide resin and acrylic resin). The conductive composition is not restricted to a specific conductive resin composition. If used to fill via holes, the conductive composition should have predetermined electrical properties. This is not even restricted to conductive

compositions. A resistor composition or thermally conductive composition can also be used if necessary.

[0028] The prepreg used as the insulator in the circuit board can be any prepreg common in the art. Specifically, a woven or unwoven fabric made of heat-resistant organic synthetic fibers such as aromatic polyamide (aramid) fibers, polyamide fibers or aromatic polyester fibers, or heat-resistant inorganic fibers such as glass fibers, is impregnated with an epoxy resin, phenol resin, polybutadiene resin, polyester resin, polyimide resin or resin combination, dried and heated to form a prepreg in which the resin is semicured. If a synthetic sheet such as a polyimide sheet, a ceramic board, or a paper phenol sheet cannot be used alone in the layers of the circuit board, a thermoplastic resin or thermocured resin can be applied to the surface of the sheet and then used as a material for circuit board connection in the present invention. The thickness of the prepreg is usually 20 to 600 μm, preferably 40 to 150 μm.

[0029] The metal foil used to form the wiring pattern is usually a foil made of copper or an alloy whose main component is copper. The thickness of the copper foil is usually 9 to 70 μm. It is usually electrolytic copper foil, but this is not a requirement. The wiring pattern can be formed using any method common in the art such as photolithography.

[0030] (2nd Embodiment)

Fig. 2 shows the circuit board configuration in the second embodiment where (a) is a cross-sectional view and (b) is an enlarged cross-sectional view of section B in (a).

[0031] In Fig. 2, 1 denotes the insulating layer which is a board consisting of an aramid unwoven fabric impregnated with epoxy resin, 2 denotes the conductive composition filling the through-holes in the insulating layer [1] which is a conductive paste consisting of copper powder mixed in with epoxy resin, 3 denotes the metal foil constituting the wiring pattern which is copper foil, and 4 denotes the conductive buffer layer which is a silver film.

[0032] The interface between the conductive buffer layer [4] and the copper foil [3] laminated on the outer surface of the outermost insulating layers [1a, 1b] is coarsened as shown in (b). In this /5 figure, only the connection interface of the copper foil on the outermost layer necessary for land strength is coarsened, but the connection interface on the inner layers can be similarly coarsened. The effect is significant when used on the shiny surfaces of the copper foil on the inner layers.

[0033] The conductive buffer layer consists of at least one metal selected from among gold, silver, tin, zinc, indium and palladium or an alloy or metal compound thereof. A metal, alloy or metal compound is formed on either the metal filler in the conductive composition or the conductive pattern.

[0034] The conductive buffer layer applies unevenness to the wiring pattern and conductive composition, increasing the contact area and number or contacts, and realizing a circuit board with superior reliability.

[0035] In the present invention, the thickness of the conductive buffer layer is preferably 0.01 to 20 μm, and more preferably 0.1 μm to 5 μm. If the conductive buffer layer is thinner than 0.1 μm, this function is not manifested. If thicker than 20 μm, the cost goes up.

[0036] (3rd Embodiment)

The following is an explanation of the circuit board manufacturing method in the third embodiment of the present invention.

[0037] Figs. 3 and 4 are cross-sectional views of the steps in the circuit board manufacturing method of this embodiment.

[0038] The insulating layer is a prepreg [1] consisting of an unwoven aramid fabric impregnated with epoxy resin. Copper foil [3] is applied to one side and a plastic film (polyethylene terephthalate PET film) [5] is applied to the other side using a laminator and press (Fig. 3 (a)).

[0039] Next, holes are formed in the prepreg [1] down to the copper foil [3] from the side with the PET film [5] using a laser, and the surface of the copper foil [3] at the bottom of the holes is abrasively finished to coarsen it using a sand blaster or jet scrubber. The holes were then filled with conductive paste [2] using the printing method (Fig. 3 (b)). Fig. 3 (b-1) is an enlarged cross-sectional view of section C in (b). As shown in this figure, the

interface between the copper foil [3] and the conductive paste [2] has been coarsened.

[0040] Next, the PET film [5] applied to the prepreg [1] filled with conductive paste is peeled off, and aligned from both sides of the core material [6] (a four-layer board in the figure) with copper foil wiring patterns [3] formed on both surfaces. It is then overlaid (Fig. 4 (c)) and clamped. In this core material [6], through-holes are formed in the predetermined positions, the through-holes are filled with conductive paste, and copper foil is laminated over the through-hole openings. A wiring pattern is then formed. These steps are repeated to complete the process.

[0041] Finally, prepregs [1] are heat pressed on both sides of the core material [6] (e.g., at 200°C under 50 Kg/cm^2 of pressure) to integrate them, and the outermost copper foil is patterned to form wiring patterns [3] (Fig. 4 (d)).

[0042] A circuit board similar to the first embodiment is obtained in this way.

[0043] (4th Embodiment)

The following is an explanation of the circuit board manufacturing method in the fourth embodiment of the present invention.

[0044] Figs. 5 and 6 are cross-sectional views of the steps in the circuit board manufacturing method of this embodiment.

[0045] The insulating layer is a prepreg [1] consisting of an unwoven aramid fabric impregnated with epoxy resin. Copper foil [3] is

applied to one side and a plastic film (polyethylene terephthalate PET film) [5] is applied to the other side using a laminator and press (Fig. 5 (a)).

[0046] Next, holes are formed in the prepreg [1] down to the copper foil [3] from the side with the PET film [5] using a laser, and the surface of the copper foil [3] at the bottom of the holes is abrasively finished to coarsen it using a sand blaster or jet scrubber. Then, a conductive buffer layer [4] such as a 3 μm silver film is formed (using the sputtering method). The holes were then filled with conductive paste [2] using the printing method (Fig. 5 (b)). Fig. 5 (b-1) is an enlarged cross-sectional view of section D in (b). As shown in this figure, the interface between the copper foil [3] and the conductive buffer layer [4] has been coarsened.

[0047] Next, the PET film [5] applied to the prepreg [1] filled with conductive paste is peeled off, and aligned from both sides of the core material [6] (a four-layer board in the figure) with copper foil wiring patterns [3] formed on both surfaces. It is then overlaid (Fig. 6 (c)) and clamped.

[0048] Finally, prepregs [1] are heat pressed on both sides of the core material [6] (e.g., at 200°C under 50 Kg/cm^2 of pressure) to integrate them, and the outermost copper foil is patterned to form wiring patterns [3] (Fig. 6 (d)).

[0049] A circuit board similar to the second embodiment is obtained in this way.

[0050] (5th Embodiment)

The following is an explanation of the circuit board manufacturing method in the fifth embodiment of the present invention.

[0051] Figs. 7 and 8 are cross-sectional views of the steps in the circuit board manufacturing method of this embodiment.

[0052] The insulating layer is a prepreg [1] consisting of an unwoven aramid fabric impregnated with epoxy resin. Through-holes are formed and filled with conductive paste [2], copper foil [3] is pressed and laminated on, and a pattern is formed in the copper foil [3]. These steps are repeated to obtain a four-layer core material [6] (Fig. 7 (a)).

[0053] Next, a prepreg [1] and PET film [5] are laminated in this order on both sides of the four-layer core material [6]. Holes are /6 formed in the prepreg [1] down to the copper foil [3] from the side with the PET film [5] using a laser, and the surface of the copper foil [3] at the bottom of the holes is abrasively finished to coarsen it using a sand blaster or jet scrubber. (Fig. 7 (b)). Fig. 7 (b-1) is an enlarged cross-sectional view of section E in (b). As shown in this figure, the surface of the copper foil [3] at the bottom of the holes [7] has been coarsened.

[0054] Next, the holes [7] are then filled with conductive paste [2] using the printing method, the PET film [5] is peeled off, copper foil is overlaid on both sides and pressed, and wiring patterns [3] are formed in the copper foil (Fig. 8 (c)). Fig. 8 (c-1) is an enlarged cross-sectional view of section F in (c).

[0055] A six-layer circuit board is obtained in this way.

[0056] (6th Embodiment)

The following is an explanation of the circuit board manufacturing method in the sixth embodiment of the present invention.

[0057] Figs. 9 and 10 are cross-sectional views of the steps in the circuit board manufacturing method of this embodiment.

[0058] The insulating layer is a prepreg [1] consisting of an unwoven aramid fabric impregnated with epoxy resin. Through-holes are formed and filled with conductive paste [2], copper foil [3] is pressed and laminated on, and a pattern is formed in the copper foil [3]. These steps are repeated to obtain a four-layer core material [6] (Fig. 9 (a)).

[0059] Next, a prepreg [1] and PET film [5] are laminated in this order on both sides of the four-layer core material [6]. Holes are formed in the prepreg [1] down to the copper foil [3] from the side with the PET film [5] using a laser, and the surface of the copper foil [3] at the bottom of the holes is abrasively finished to coarsen it using a sand blaster or jet scrubber. (Fig. 7 (b)). Fig. 7 (b-1) is an enlarged cross-sectional view of section G in (b). As shown in this figure, the surface of the copper foil [3] at the bottom of the holes [7] has been coarsened.

[0060] Next, a conductive buffer layer [4] such as a 3 μm silver film is formed (using the sputtering method). The holes are then filled with conductive paste [2] using the printing method, the PET film [5] is peeled off, copper foil is overlaid on both sides and

pressed, and wiring patterns [3] are formed in the copper foil (Fig. 10 (c)). Fig. 10 (c-1) is an enlarged cross-sectional view of section H in (c).

[0061] The conductive buffer layer consists of at least one metal selected from among gold, silver, tin, zinc, indium and palladium or an alloy or metal compound thereof. A metal, alloy or metal compound is formed on either the metal filler in the conductive composition or the conductive pattern.

[0062] The conductive buffer layer applies unevenness to the wiring pattern and conductive composition. This increases the contact area and number of contact points to realize a circuit board with superior reliability.

[0063] The circuit boards obtained in these embodiments obtained good results in CSP package and MCM environmental tests. There were no connection defects in thermal impact and PCT (pressure cutter test) tests, and the rate of change in the resistance was lower than in the prior art.

[0064] [Effect of the Invention]

As explained above, the contact interface between the wiring pattern and conductive composition is coarsened in the circuit board of the present invention, or a conductive buffer layer is formed between the wiring pattern and the conductive composition and the contact interface between the wiring pattern and the conductive buffer layer is coarsened. This obtained good results in CSP package and MCM environmental tests. There were no connection defects in thermal

impact and PCT (pressure cutter test) tests, and the rate of change in the resistance was lower than in the prior art.

[0065] Because the coarsened region of the wiring pattern was limited to the connection interface with the conductive composition or conductive buffer layer, it was easier to form a fine pattern in the wiring pattern than when the entire surface is coarsened.

[0066] The circuit board manufacturing method of the present invention is able to efficiently manufacture a circuit board with these effects.

[Brief Explanation of the Invention]

[Figure 1] A views of the steps in the circuit board manufacturing method of the first embodiment where (a) is a cross-sectional view and (b) is an enlarged cross-sectional view of section A in (a).

[Figure 2] A views of the steps in the circuit board manufacturing method of the second embodiment where (a) is a cross-sectional view and (b) is an enlarged cross-sectional view of section B in (a).

[Figure 3] A cross-sectional view of the steps in the circuit board manufacturing method of the third embodiment.

[Figure 4] A cross-sectional view of the steps in the circuit board manufacturing method of the third embodiment.

[Figure 5] A cross-sectional view of the steps in the circuit board manufacturing method of the fourth embodiment.

[Figure 6] A cross-sectional view of the steps in the circuit board manufacturing method of the fourth embodiment.

[Figure 7] A cross-sectional view of the steps in the circuit board manufacturing method of the fifth embodiment.

[Figure 8] A cross-sectional view of the steps in the circuit board manufacturing method of the fifth embodiment.

[Figure 9] A cross-sectional view of the steps in the circuit board manufacturing method of the sixth embodiment.

[Figure 10] A cross-sectional view of the steps in the circuit board manufacturing method of the sixth embodiment.

[Key to the Drawings]

1 Insulating Layer (Prepreg Sheet)

2 Conductive Composition (Conductive Paste)

3 Wiring Pattern (Copper Foil)

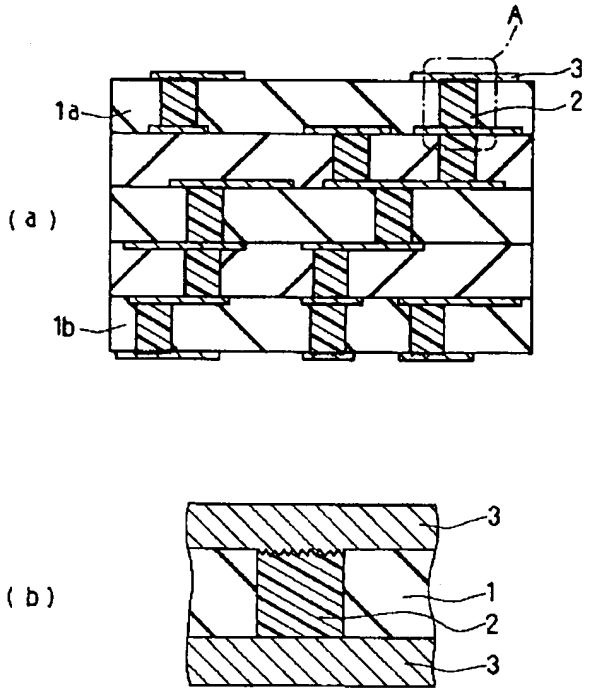
4 Conductive Buffer Layer /7

5 Plastic Film (PET Film)

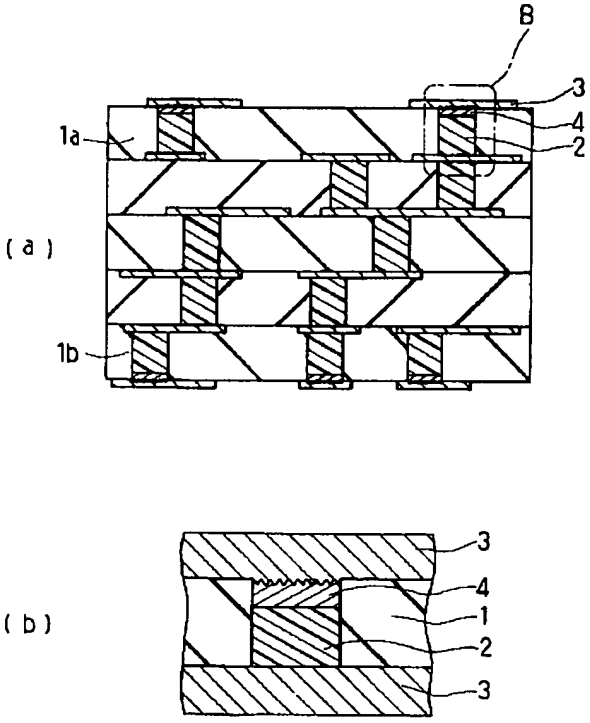
6 Core Material

7 Hole

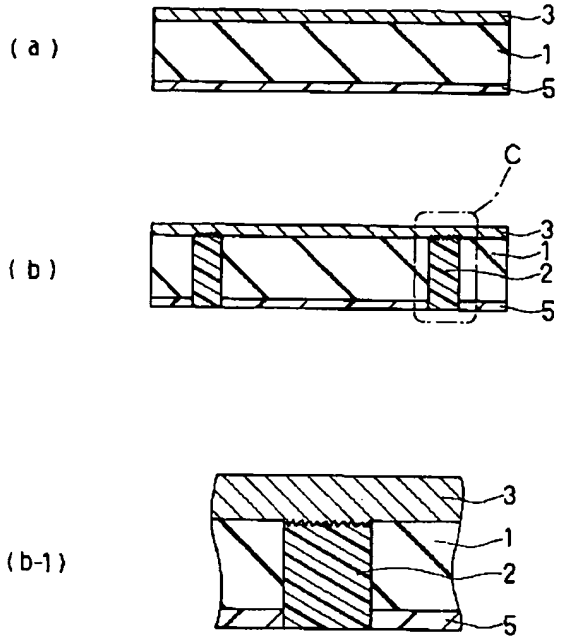
[Figure 1]



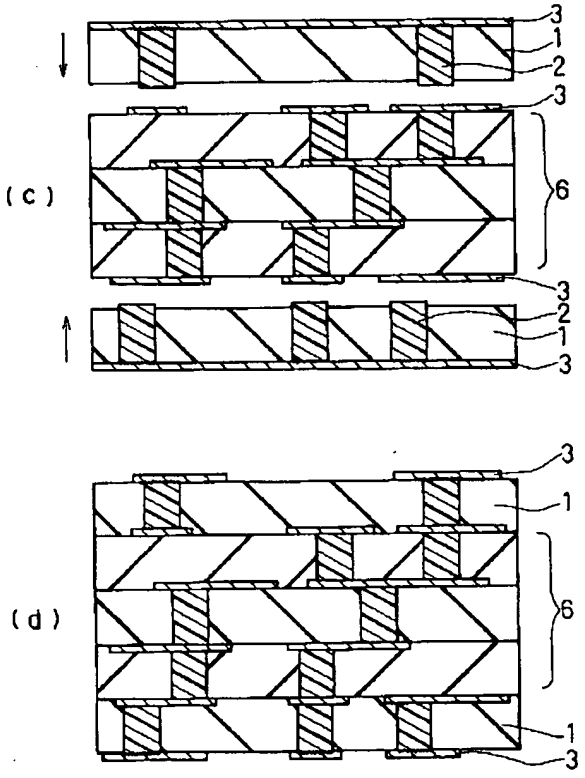
[Figure 2]



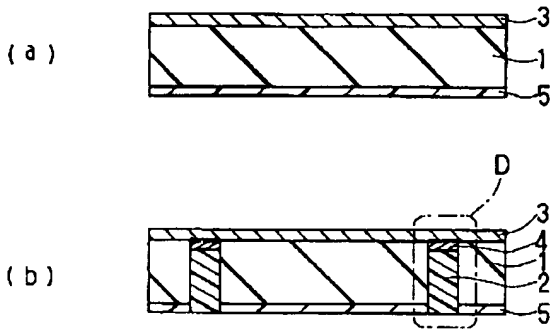
[Figure 3]



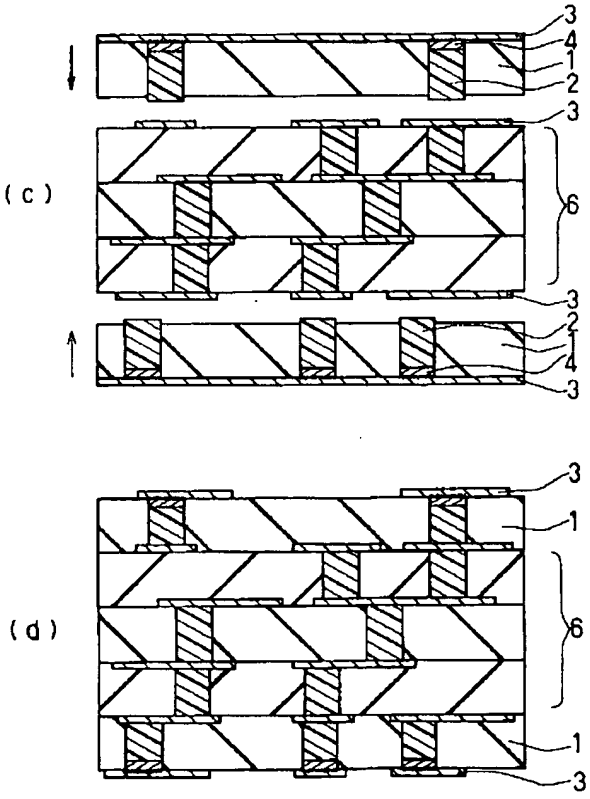
[Figure 4]



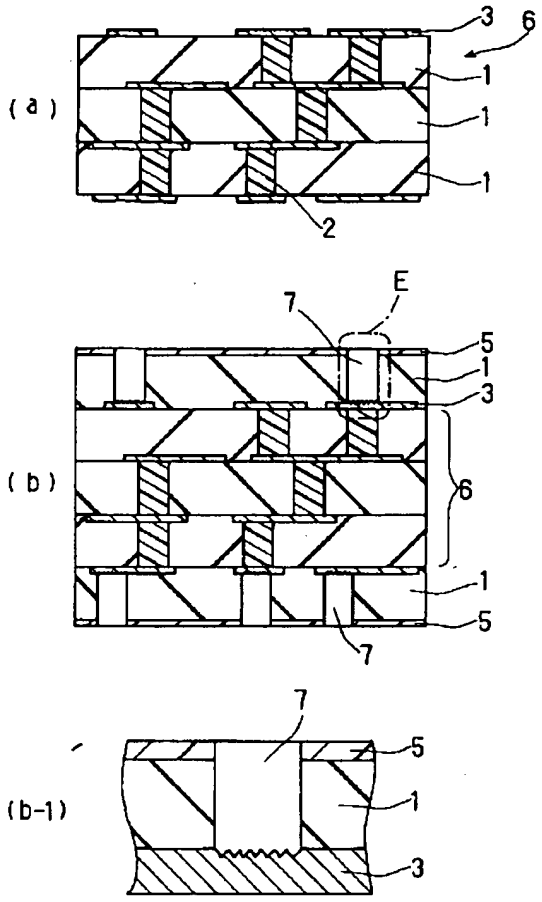
[Figure 5]



[Figure 6]

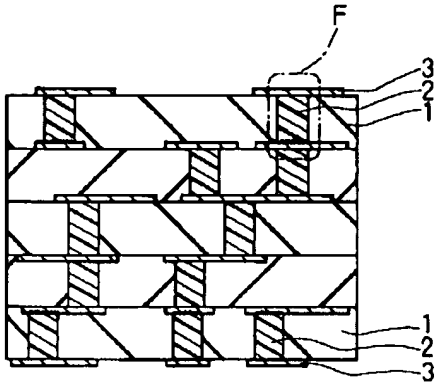


[Figure 7]

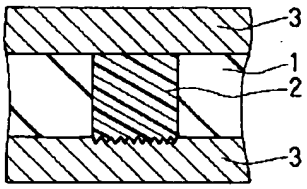


[Figure 8]

(c)

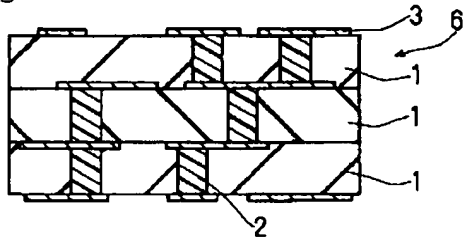


(c-1)

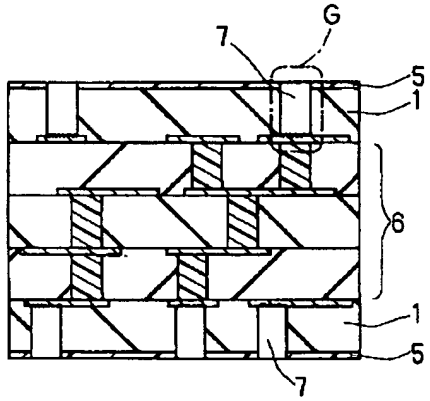


[Figure 9]

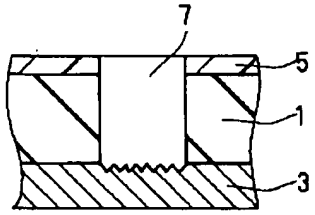
(a)



(b)

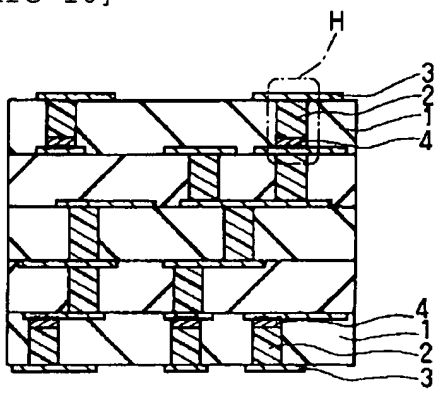


(b-1)



[Figure 10]

(c)



(c-1)